PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re application of: Alan Folmsbee | Group Art Unit: 2132 |
| | Examiner: Lanier, B.E. |
| Application No.: 09/376,654 | Atty. Docket No.: SUNMP210 |
| Filed: August 18, 1999 | Date: October 17, 2006 |
| For: SECURE PROGRAM EXECUTION DEPENDING ON PREDICTABLE ERROR CORRECTION | |

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 17, 2006.

Signed: _____
Sylvia Castillo

**RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF (37 CFR 41.37)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice of Non-Compliant Appeal Brief (37 CFR 41.37) dated October 4, 2006, which was issued by the United States Patent and Trademark Office, Applicant hereby attaches a 2nd Replacement Supplemental Appeal Brief. A copy of the Notification is being returned with this response.

Applicant believe no charges are due in connection with the submission of these papers, however the Commissioner is authorized to charge any other fees that may be due to our Deposit Account No. 50-0805 (Order No. SUNMP210).

Respectfully submitted,
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application for Patent

FOR:

# SECURE PROGRAM EXECUTION DEPENDING ON PREDICTABLE ERROR CORRECTION

# 2nd REPLACEMENT SUPPLEMENTAL APPEAL BRIEF

**EX PARTE Alan C. Folmsbee**

**Application No. 09/376,654**
**Filed August 18, 1999**
**Technology Center/Art Unit 2132**

Submitted in accordance with 37 C.F.R. §41.67

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Signed: _____
Sylvia Castillo

MARTINE PENILLA & GENCARELLA, LLP
Attorneys for Appellant

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## I. REAL PARTY IN INTEREST

The real party in interest is Sun Microsystems, Inc., the assignee of the present application.

## II. RELATED APPEALS AND INTERFERENCES

The undersigned is not aware of any related appeals or interferences.

## III. STATUS OF THE CLAIMS

Claims 1, 3, 4, 13, 17, and 18 are pending in the subject application; claims 2, 5-12, 14-16, and 19-26 are canceled. Claims 1, 3, 4, 13, 17, and 18 have been rejected in the Office Action of June 14, 2005, which reopened prosecution following Appellant's submission of the previous Appeal Brief. The Office Action of June 14, 2005 withdrew all previous rejections and applied new rejections based on newly cited art. The Supplemental Appeal Brief submitted on September 2, 2006 was Appellant's first opportunity to respond to the currently outstanding rejections. This 2nd Replacement Supplemental Appeal Brief is filed in response to the second Notice of Non-Compliance mailed from the PTO on October 4, 2006.

## IV. STATUS OF THE AMENDMENTS

No amendments, cancellations or other changes have been made after the Final Office Action of December 15, 2004.

## V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates to a microprocessor for executing computer instructions. The microprocessor presently disclosed is modified from a typical microprocessor in that it includes a number of security enhancements. The security enhancements allow the microprocessor to execute code that will not execute on other processors. Thus, the software must be specifically modified for the particular processor and, once modified, will not run on other processors. Since the software will not run on other processors the problem of software piracy is effectively addressed. The processor is further designed to obfuscate the specific modifications and make reverse engineering difficult.

**A. Claim 1 sets forth the following features represented by way of example in the specification and drawings:**

| | |
|---|---|
| A particularly configurable processor for processing error induced computer programs which are selectively operable on said particularly configurable processor, comprising: | Figure 1, CPU 11; Figure 11, CPU 161; page 5 lines 12-14; page 22, lines 7-17. |
| a central processing unit chip; | Figure 1, CPU 11; Figure 11, CPU 161; page 5, lines 12-14; page 22, lines 10-13, line 17. |
| processor circuitry on said chip; | Figure 1, logic 13; page 25, lines 28-33. |
| a programmable error correcting circuit on said chip; | Figure 11, circuitry 169; page 22, lines 17-20. |
| RAM on said chip storing error correcting information, said RAM being in communication with said programmable error correcting circuit; and wherein | Figure 11, registers 165; page 22, lines 17-21. |
| the programmable error correcting circuit receives said error correcting information and processor instructions containing errors that are not capable of being executed by said processing circuitry, and | Figure 11, circuitry 169; page 22, lines 13-16; page 22, lines 19-21. |
| said programmable error correcting circuit generates corrected processor instructions in response to said processor instructions containing errors and said error correcting information, the corrected processor instructions being capable of being executed by said processing circuitry. | Figure 1, logic 13; Figure 11, circuitry block 173; page 22, lines 8-10 and 19-22; page 25, lines 30-32. |

**B. Claim 17 sets forth the following features represented by way of example in the specification and drawings:**

| | |
|---|---|
| A microprocessor for processing computer programs which are selectively operable on selected ones of individual microprocessors, comprising: | Figure 1, CPU 11; Figure 11, CPU 161; page 5 lines 12-14; page 22, lines 7-17. |
| an integrated circuit chip; | Figure 1, CPU 11; Figure 11, CPU 161; page 5, lines 12-14; page 22, lines 10-13, line 17. |
| instruction processing circuits on said chip; | Figure 1, logic 13; page 25, lines 28-33. |
| a programmable error correcting circuit on said chip; and | Figure 11, circuitry 169; page 22, lines 17-20. |
| a memory location for storing error correction information, said programmable error correction circuit selecting an error correction scheme based on said error correction information; and | Figure 11, registers 165; page 22, lines 17-21. |
| wherein said programmable error correcting circuit receives instructions having errors and said error correction information, and said instruction processing circuits process corrected instructions generated by said programmable error correcting circuit. | Figure 1, logic 13; Figure 11, circuitry block 173; page 22, lines 8-10 and 19-22; page 25, lines 30-32. |

**C. Claim 18 sets forth the following features represented by way of example in the specification and drawings:**

| | |
|---|---|
| A method for processing a computer program on a microprocessor, the method comprising: | Figure 1, CPU 11; Figure 11, CPU 161; page 5 lines 12-14; page 22, lines 7-17. |
| intentionally placing errors in the computer program; | Figure 11, block 171; page 22, lines 8-10 and 19-21. |

| | |
|---|---|
| loading instructions of said computer program onto instruction registers on a microprocessor chip; | Figure 2, registers 53, 55, 57; page 7, lines 2-5; page 22, lines 19-21. |
| storing error correction control information on said chip; | Figure 11, registers 165; page 22, lines 17-19; |
| on said chip, correcting said instructions using said error correction control information; | Figure 11, blocks 169, 173; page 22, lines 19-21. |
| and executing said instructions on said chip. | Figure 1, logic 13; Figure 11, circuitry block 173; page 22, lines 21-22; page 25, lines 30-32. |

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds for rejection to be reviewed on appeal are as follows:

(1) claim 4 is rejected under 35 U.S.C. § 112, second paragraph, and

(2) claims 1, 3, 4, 13, 17, and 18 are rejected under 35 U.S.C. § 102(e) for being anticipated by U.S. Patent 6,044,483 issued to Chen et al. (Chen).

## VII. ARGUMENTS

In the discussion below, all references to "the Office Action" will be made, unless otherwise noted, to the most recent (non-final) Office Action mailed June 14, 2005. All references to the claims and to specific lines in the claims will be made in reference to the claims in the attached claim listing (section VIII). When line numbers are mentioned, unless the source document already has line numberings (e.g., an issued patent) every printed line is counted including any headings, but not including any page headers.

**ISSUE 1: Whether claim 4 is indefinite under 35 U.S.C. § 112, second paragraph.**

Claim 4 is rejected under 35 U.S.C. § 112, second paragraph, for being indefinite. Specifically, the Office Action states that "the limitation 'the error correction key' in line 3" lacks antecedent basis.

Appellant agrees with the Examiner's position with regard to Issue 1.

**ISSUE 2: Whether claims 1, 3, 4, 13, 17, and 18 are anticipated by Chen.**

Claims 1, 3, 4, 13, 17, and 18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Chen. Appellant traverses because Chen does not disclose each and every element of the invention as set forth in the claims.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See MPEP 2131. Therefore, the presence of a single claim element not disclosed by the prior art reference cited in the rejection is sufficient to overcome an anticipation rejection under 35 U.S.C. § 102. There are many differences between the claimed invention and Kobus; the claim elements mentioned in the following discussion are presented as examples only of the many differences wherein each difference is sufficient to overcome the anticipation rejection.

There are many distinguishing features set forth in the claims that are not disclosed by Chen.

Claim 1 sets forth, "a central processor unit chip" and "processor circuitry on said chip" (line 4) and "a programmable error correcting circuit on said chip" (line 5) wherein "the programmable error correcting circuit receives said . . . processor instructions containing errors" (lines 9-10) and "the corrected processor instructions being capable of being executed by said processing circuitry" (lines 14-15). Chen does not disclose a central processor unit chip having processor circuitry. Chen discloses a dual in-line memory device (DIMM) having a plurality of memory chips and an error correction code (ECC) circuit (col. 4, lines 42-46; col. 7, lines 4-7; Figure 1, element 101 ("DIMM"), element 103 ("ECC LOGIC"), and element 102 ("MEMORY CHIPS"). Chen's contribution is providing an application specific integrated circuit (ASIC) chip on the memory module for performing error correction for data stored on the memory chips. See Col. 4, lines 41-46. Chen does not disclose a processor capable of executing corrected processor instructions on the ASIC chip, the memory chips, or on the memory module. The Office Action refers only to Figure 7 of Chen, as meeting these limitations (Office Action, page 3, lines 21-26). Appellant has carefully reviewed Figure 7 of Chen, and in fact has read the entire disclosure, but could find no suggestion that supports the Office's conclusory statements regarding these limitations. Appellant therefore respectfully requests that the 35 U.S.C. § 102(e) rejection be REVERSED and that claims 1, 3 and 13 be ALLOWED.

Claim 1 also sets forth "RAM on said chip storing error correcting information" (line 7). RAM stands for "random access memory" (see, e.g., the Application as originally filed, page 12, line 22). Chen does not disclose RAM on the chip. Chen teaches a memory module comprising an ASIC chip for performing error correction and a plurality of memory chips. See Figure 1, element 101 ("DIMM"), element 103 ("ECC LOGIC"), and element 102 ("MEMORY CHIPS"). There is no mention of any RAM on the ASIC chip or RAM for storing error correcting information. Since Chen does not disclose "RAM on said chip for storing error correcting information" Appellant respectfully submits that Chen does not anticipate claim 1. Appellant therefore respectfully requests that the 35 U.S.C. § 102(e) rejection be REVERSED and that claims 1, 3, 4, and 13 be ALLOWED.

Dependent claims 3, 4, and 13 depend from claim 1 and further define and distinguish the invention from the prior art, thereby giving rise to separate reasons for allowability. For example, claim 3 sets forth that "error correcting information includes a key that enables selection of error correction specific to an error scheme used to generate said errors" (claim 3, lines 1-3). The Office Action mentions that Chen discloses a concept of intentionally introducing an error of a type recognizable by a host computer system, and states that this "meets the limitation of said error correcting information includes a key. . ." (page 4, lines 1-10). Appellant respectfully disagrees. While Chen does teach intentionally introducing an error into a corrected data word so that the host system can correct and, more importantly, log the error, Chen does not mention a programmable error correcting circuit that receives error correcting information and processor instructions containing errors (claim 1, lines 9-10) wherein the error correcting information comprises a key which enables selection of error correction specific to an error correction scheme used to generate the errors (claim 3, lines 1-3). Nor does Chen disclose "wherein instructions provided to said processor include an intentional introduction of errors which are correctable with error correction algorithms, said correction algorithms pre-selected according to the key" (claim 13, lines 1-3). Chen does not provide a key to the microprocessor along with corrected data (which is not even disclosed by Chen as including instructions). Thus, even if Chen taught selecting a correction algorithm, which Chen does not, it does not provide the basic features set forth in the claims of a processor receiving a key and error-encoded instructions. Chen does not show the processor as having a programmable error correcting circuit responsive to the key and the error-encoded instructions. Chen does not teach correcting the instructions and executing the instructions on

a single chip. Since dependent claim 3, 4, and 13 further distinguish from Chen, Appellant respectfully asserts that they do not anticipate Chen for reasons beyond the depended-upon claim 1, discussed above.

Claim 17 sets forth a microprocessor. Chen does not teach a microprocessor. Instead, Chen teaches a memory module having memory chips and an ASIC chip for correcting errors in data stored by the memory chips. See Figure 1; col. 4, lines 42-46; col. 6 lines 50-54; col. 7, lines 4-22. Chen does teach that this memory module may cooperate with a host computer system, which presumably has a microprocessor and may have existing error correcting circuitry. However, there is no mention that the error correcting circuitry of the host computer system is programmable (claim 17, line 5), that the error correcting circuitry is on the same chip as the microprocessor (claim 17, lines 4-5), or that the error correcting circuitry on the host computer system selects an error correction scheme based error correction information (claim 17, lines 6-8). The ASIC chip disclosed by Chen which does have error correcting circuitry is not capable of processing instructions (claim 17, line 4) nor does it include a memory location for storing error correction information such that the programmable error correction circuit selects an error correction scheme based on the error correction information (claim 17, lines 6-8). Chen does teach a mode selection so that error correction can be based on either 4 bits per chip data storage or 8 bits per chip. However, Chen enables the selection by tying a pin to Vcc or ground at the time it is manufactured (col. 7, lines 46-57). The Office Action does not provide any details as to how Chen meets the limitations of claim 17 other than what has already been addressed above. Since Chen does not show each and every limitation set forth in claim 17, Appellant respectfully submits that Chen does not anticipate claim 17. Appellant therefore respectfully requests that the 35 U.S.C. § 102(e) rejection be REVERSED and that claim 17 be ALLOWED.

Claim 18 sets forth a method for processing a computer program. Chen does not mention processing a computer program. Chen discloses a memory module having an ASIC chip for correcting errors in data stored on a plurality of memory chips. See Figure 1; col. 4, lines 42-46; col. 6 lines 50-54; col. 7, lines 4-22. Chen does not mention executing instructions. Chen does teach that this memory module may cooperate with a host computer system, which presumably has a microprocessor and may have existing error correcting circuitry. However, there is no mention of storing error correction control information on the host computer's microprocessor chip (claim 18, line 6) or of correcting the instructions on the

host computer microprocessor chip (claim 18, line 7) using the error correction control information (claim 18, lines 7-8). Chen does teach an ASIC chip for correcting errors on the memory module (col. 7, lines 4-22). However, there is no mention of this ASIC chip being capable of executing instructions (claim 18, line 9). While Chen does mention intentionally inserting an error in a corrected data word (col. 25, lines 29-32) Chen does not mention intentionally placing errors in a computer program (claim 18, line 3), loading instructions of the computer program onto instruction registers of a microprocessor chip (claim 18, lines 4-5), storing error control information on the chip (claim 18, line 6), correcting the instructions on the chip using the error control information (claim 18, lines 7-8) or executing the instructions on the chip (claim 18, line 9). Since Chen does not disclose each and every limitation set forth in claim 18, Appellant respectfully submits that claim 18 is not anticipated by Chen. Appellant therefore respectfully requests that the 35 U.S.C. § 102(e) rejection be REVERSED and that claim 18 be ALLOWED.

For all the foregoing reasons, the rejection of claims 1, 3, 13, 17, and 18 under 35 U.S.C. §102(e) as being anticipated is improper and should be reversed. Accordingly, Appellant respectfully submits that the anticipation rejection is in error, and requests that the Board of Patent Appeals and Interferences reverse this rejection on appeal.

Respectfully submitted,
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# VIII. CLAIMS APPENDIX

## CLAIMS ON APPEAL

1. A particularly configurable processor for processing error induced computer programs which are selectively operable on said particularly configurable processor, comprising:

a central processing unit chip;

processor circuitry on said chip;

a programmable error correcting circuit on said chip;

RAM on said chip storing error correcting information, said RAM being in communication with said programmable error correcting circuit; and wherein:

the programmable error correcting circuit receives said error correcting information and processor instructions containing errors that are not capable of being executed by said processing circuitry, and

said programmable error correcting circuit generates corrected processor instructions in response to said processor instructions containing errors and said error correcting information, the corrected processor instructions being capable of being executed by said processing circuitry.

3. The processor of claim 1, wherein said error correcting information includes a key that enables selection of error correction specific to an error scheme used to generate said errors.

4. The processor of claim 1, wherein information provided in compiled computer program data in part controls said error correction, thereby providing complementary error correction with a combination of the error correction key and the information provided in the compiled computer program data.

13. The processor of claim 3, wherein instructions provided to said processor include an intentional introduction of errors which are correctable with error correction algorithms, said correction algorithms pre-selected according to the key.

17. A microprocessor for processing computer programs which are selectively operable on selected ones of individual microprocessors, comprising:

an integrated circuit chip;

instruction processing circuits on said chip;

a programmable error correcting circuit on said chip; and

a memory location for storing error correction information, said programmable error correction circuit selecting an error correction scheme based on said error correction information; and

wherein said programmable error correcting circuit receives instructions having errors and said error correction information, and said instruction processing circuits process corrected instructions generated by said programmable error correcting circuit.

18. A method for processing a computer program on a microprocessor, the method comprising:

intentionally placing errors in the computer program;

loading instructions of said computer program onto instruction registers on a microprocessor chip;

storing error correction control information on said chip;

on said chip, correcting said instructions using said error correction control information; and

executing said instructions on said chip.

## IX. EVIDENCE APPENDIX

None.

## X. RELATED PROCEEDINGS APPENDIX

None.